REMARKS/ARGUMENTS

In response to the Office Action dated March 24, 2004, claims 1 and 2 are amended. Claims 4-13 were canceled without prejudice or waiver. Claims 1-3 remain in the application. It is not the Applicants' intent to surrender any equivalents because of the amendments or arguments made herein. Reconsideration of the application, and entrance of these amendments, are respectfully requested.

Claim Objections

In paragraph 3 of the Office Action, claims 2 and 3 were objected to for informalities, namely, claim 2 having grammatical and punctuation errors.

The Applicant thanks the Examiner and has amended the claims to overcome the objections. The Applicant believes that these amendments merely clarify the claim language, and, as such, the Applicant does not intend to surrender any equivalents because of these amendments.

Non-Art-Based Rejections

In paragraph 4 of the Office Action, claim 1 was rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The Applicant thanks the Examiner and has amended the claim to overcome the rejection.

Art-Based Rejections

In paragraph 5 of the Office Action, claims 1-2 were rejected under 35 U.S.C. § 102(e) as being anticipated by Shinozuka, USPN 6,560,200.

The Applicant respectfully traverses the rejections and respectfully submit that the claims are patentable in light of the arguments below.

The Shinozuka Reference

The Shinozuka reference discloses a serial bus experimental apparatus. The controller 3n instructs the link layer circuit 5n to transmit a packet for a desired node instrument or to receive a packet from a desired node instrument. Further, according to the instruction through the operational panel 12, the controller 3n allows the display of a reception packet stored in the memory 10 on the display device 11. Still further, the controller 3n sets a reference packet to the reference packet set up circuit 27 in the packet capture circuit 32, and instructs the capture control circuit to start or stop capturing. See Col. 10, lines 46-58.

The Claims are Patentable over the Cited Reference

The claims of the present invention describe a method and device for testing a physical layer. A method in accordance with the present invention includes a link layer interface, a physical layer logic circuit to be connected to said link layer interface, and a plurality of ports to be connected to said physical layer logic circuit are provided beforehand in said physical layer device, where in testing, a test link layer circuit is connected to said physical layer logic circuit through said link layer interface, and a test physical layer logic circuit is connected to a first port that is one of said plurality of ports, and said first port is connected to a second port that is one of said plurality of ports through an external bus, and the second port is connected to said physical layer logic circuit; and said link layer interface, said physical layer logic circuit, and said plurality of ports are tested.

The cited reference does not teach nor suggest the limitations of the claims of the present invention. Specifically, the cited reference does not teach nor suggest the limitation of said first port is connected to a second port that is one of said plurality of ports through an external bus, and the second port is connected to said physical layer logic circuit as described in the claims of the present invention.

The Shinozuka reference describes a device similar to that is described in FIG. 5 of the application. Shinozuka requires that a second device, namely, device 2n, be connected to the ports of the physical layer device being tested as well as to another link layer device.

Shinozuka does not recognize that the ports of the physical layer device being tested can be connected through an external bus, and that one of the ports of the physical layer device being tested can be connected to another port of the same device, e.g., ports 1i-1 and 1i, as part of instrument 2i of Shinozuka.

Shinozuka merely teaches that an additional testing device, namely, device 2n, can be used to test device 2i. Shinozuka teaches that a first physical layer 4n is connected to a second physical layer 4i. Shinozuka does not teach nor suggest that physical layer 4i is connected to itself by connection ports 1i-1 to 1i, for testing purposes.

As such, Shinozuka does not teach nor suggest at least the limitation of a first port that is one of said plurality of ports, being connected to a second port that is one of said plurality of ports through an external bus, and the second port is connected to the physical layer logic circuit as recited in the claims of the present invention.

Thus, it is submitted that independent claims 1 and 2 are patentable over the cited reference. Claim 3 is also patentable over the cited reference, not only because they contain all of the limitations of the independent claim, but because claim 3 also

describe additional novel elements and features that are not described in the prior art.

Conclusion

In view of the foregoing, it is respectfully submitted that the application is in condition for allowance. Reexamination and reconsideration of the application, as amended, are requested.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at the Los Angeles, California telephone number (213) 337-6742 to discuss the steps necessary for placing the application in condition for allowance.

If there are any fees due in connection with the filing of this response, please charge the fees to our Deposit Account No. 50-1314.

Respectfully submitted,
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Date: July 26, 2004

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